**19EC3202 – VLSI DESIGN**

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| **Course category:** | Program Elective | **Credits:** | 3 |
| **Course Type:** | Theory |  **Lecture - Tutorial - Practical:** | 3 - 0- 0 |
| **Prerequisite:** | Electronic Devices & Circuits, Linear & Digital ICs and Basics of IC Fabrication | **Sessional Evaluation :****External Evaluation:****Total Marks:** | 4060100 |
| **Course****Objectives** | Students undergoing this course are expected: |
| 1. To introduce the fundamental structures of VLSI Systems at the lowest levels of  System abstraction.2. To know the basic electrical properties of MOS & BI-CMOS circuits3. To understand the Basic Circuit Concepts and design process of VLSI circuits and also to introduce the fundamental principles of VLSI circuit design.4. To know the Gate level design and physical design by considering partioning, floor  Planning, Placement and Routing.5. To bring both Circuits and System views on design together by considering circuit  Subsystems and VLSI Design styles. 6. To have a profound understanding of the design of complex digital VLSI circuits,  computer aided simulation and synthesis tool for  hardware design |
| **Course Outcomes** | Upon successful completion of the course , the students will be able to: |
| **CO1** | Know the trends in semiconductor technology, and how it impacts scaling and performance. |
| **CO2** | analyze the basic electrical characterstics of MOS & BI-CMOS circuits |
| **CO3** | Learn Layout, Stick diagrams, Fabrication steps, Static and Switching characteristics of inverters |
| **CO4** | Estimate delay in circuits and knows routing techniques for clock and power |
| **CO5** | Understand design styles in VLSI like full-custom, FPGA etc. |
| **CO6** | Discriminate various faults in circuits and to develop fault-modeling synthesis. |
| **Course****Content****Course****Content** | **UNIT-I****INTRODUCTION:** IC fabrication - MOS, PMOS, NMOS, CMOS & Bi-CMOS Technologies - Oxidation, Lithography, Diffusion, Ion implantation, Metallization, Encapsulation, Probe testing, Integrated Resistors and capacitors.**UNIT-II****BASIC ELECTRICAL PROPERTIES OF MOS & Bi-CMOS CIRCUITS:** Ids-Vds relationships, MOSFET threshold voltage, gm, gds, ωo, Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design Bi-CMOS inverters.**UNIT-III****BASIC CIRCUIT CONCEPTS:** Sheet Resistance Rsand its concepts to MOS, Area Capacitance calculations, Inverter Delays, Driving large Capacitive Loads, Wiring Capacitances, Fan-In and Fan-Out.**VLSI CIRCUIT DESIGN PROCESSES:** VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, 2µm CMOS Design rules for wires, Contacts and Transistors, Layout Diagrams for NMOS and CMOS Inverters and gates , Scaling of MOS circuits, Limitation of Scaling.**UNIT-IV****GATE LEVEL DESIGN:**  Logic gates and other Complex gates, Switch Logic, Alternate Gate circuits.**PHYSICAL DESIGN:**  Floor- Planning, Placement, routing, Power delay estimation, Clock and Power routing **UNIT-V****SUBSYSTEM DESIGN:** Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Counters, High density Memory Elements.**VLSI DESIGN STYLES:** Full-custom, Standard Cells, Gate-arrays, FPGAs and CPLDs and Design approach for Full Custom and Semi-Custom devices.**UNIT-VI****VHDL Synthesis:** VHDL Synthesis, Circuit Design Flow, Circuit Synthesis, Simulation, Layout, Design capture tools, Design Verification Tools.**TEST AND TESTABILITY:** Fault-modelling and simulation, test generation, design for testability, Built-in self-test. |
| **Text Books and Reference Books** | **TEXT BOOKS:**1. Essentials of VLSI circuits and Systems – Kamran Eshraghian, Eshraghian Douglas and A. Pucknell, PHI, 2005 Edition.
2. Principles of CMOS VLSI Design- Weste and Eshraghian, Pearson Education,1999
3. ASIC Design Flow by Smith.

**REFERENCE BOOKS:**1. D. Roy Chowdhury. Linear Integrated circuits, New Age International Edition(2003)
2. Modern VLSI Design-Wayne Wolf, Pearson Education, 3rd Edition 1997.
3. Introduction to VLSI Circuits and Systems – John. P. Uyemura. John Wiley, 2003.
4. Digital Integrated Circuits – John M. Rabaey, PHI.
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| **E-Resources** | 1. http://nptel.ac.in/courses
2. http://tocs.ulb.tu-darmstadt.de/35621702.pdf
3. http://www.ulb.tu-darmstadt.de/tocs/23570458.pdf
4. http://www.academia.edu/download/30922844/L1-print.pdf
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| **Contribution of Course Outcomes towards achievement of Program Outcomes** |
|  | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
| CO1 | 3 | 3 | 2 | 2 | 1 | - | - | - | - | - | - | 2 | 3 | 3 |
| CO2 | 3 | 3 | 2 | 2 | 1 | - | - | - | - | - | - | 2 | 3 | 2 |
| CO3 | 3 | 3 | 3 | 1 | 1 | - | 1 | - | - | 1 | - | 2 | 2 | 3 |
| CO4 | 3 | 3 | 2 | 2 | 1 | - | 1 | - | - | 1 | - | 2 | 2 | 3 |
| CO5 | 3 | 3 | 2 | 2 | 1 | 1 | 1 | - | - | 1 | - | 2 | 3 | 2 |
| CO6 | 3 | 3 | 2 | 2 | 1 | 1 | - | - | - | - | - | 2 | 3 | 2 |